REMARKS

Claims 1-13, 21-37 and 39-44 are pending in the present application. Claims 14-20 were previously canceled and claim 38 is canceled herein. Claims 1, 21-23, 28, 30, 31, 36, 37, 41 and 44 have been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

The drawings are objected to because the graph in Fig. 8 is labeled in German. Applicant has translated the German labeling of Figure 8 into English and provides a corrected replacement sheet of Figure 8.

Claims 1, 21, 22, 28, 30 and 41 are objected to because of informalities. Applicant has amended claims 1, 21, 22, 28, 30 and 41 to comply with the Examiner's request so that the objection is now moot.

Claims 23 and 44 are rejected under 32 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 23 and 44 in order to comply with the Examiner's request.

Claim 21 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner found that "area selective etching to increase the structure size of the trench structures" is unclear. According to the Examiner, it is especially not clear whether the phrase means "selectively expand every trench" or "expanding only selected trenches." Applicant respectfully disagrees. Claim 21 specifically recites in line 11 "of the trench structures." Clearly, this recitation refers to the trench structures in the preamble and

therefore to all trench structures. Applicant respectfully requests that Examiner withdraw this rejection.

Claim 21 is further rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner found that the term "secondary structure" appears without reference to any structure described as a primary structure. Applicant respectfully disagrees. "Secondary structure" is described in the published application in paragraphs [0039], [0056]-[0060] and [0064], for example. For example, secondary structures 132 are essentially arranged in a section of the semiconductor substrate 6 near the surface, between the surface of the semiconductor substrate 6 and a structure edge in the depth or the semiconductor substrate. By contrast, substantial parts of the main structure 131 are formed below the structure edge (see paragraph [0058]). In one embodiment, paragraph [0077] describes the secondary structure as selection transistor assigned to a storage capacitance. Hence, secondary structure appears with reference to a structure described as a primary structure and Applicant requests that Examiner withdraw this rejection. Claims 2-13 are not indefinite because claim 21 is not indefinite.

Claims 1, 22, 23 and 27 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka et al. (U.S. Patent Publication No. 2001/0016398, hereinafter "Kudelka") in view of Yasue (JP 05/109984, hereinafter "Yasue"). Claims 24, 25 and 26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka and Yasue as applied to claim 1, and further in view of Endoh et al. (U.S. Patent No. 7,141,506, hereinafter "Endoh"). Applicant respectfully traverses these rejections.

Claim 1, as amended, recites "etching a surface opening of said trench structures in said first areas, wherein the upper portion of the trench structure comprises sidewalls substantially

parallel to the crystal faces that are less resistant to etching, and etching said lower portion of the trench structures in order to form sidewalls which are substantially parallel to the crystal faces that are more resistant to etching." Kudelka, either singly or in combination with Yasue, does not teach or suggest such a method.

The Examiner states that Kudelka defines a grid with respect to the <110> orientation but Kudelka does not contain the step of defining a grid with respect to the <100> crystal orientation (see Office Action mailed July 30, 2009, page 9). However, the Examiner is under the impression that, since Yasue discloses that the <100> crystal orientation is more desirable for oxide films than the <110> crystal orientation, a person skilled in the art would have combined the teachings of Kudelka and Yasue to arrive at the claimed limitation (see Office Action, page 10). Applicant respectfully disagrees.

Kudelka teaches a trench with sidewalls along the crystal face <110> (see paragraph [0044]; Figures 11, 15-16). Kudelka further teaches that silicon surfaces are etched faster in <100> direction than in <110> direction (see paragraph [0044]).

Yasue teaches that the oxidization speed between <100> and <110> differs on a semiconductor surface and that it is more desirable to have <100> sides than <110> sides (see paragraph [0019]); Abstract).

A person skilled in the art would not have combined the teachings of Kudelka with those of Yasue. Kudelka teaches *etching* crystal faces and Yasue teaches *oxidizing* crystal faces. Etching is a different process than oxidizing and what is true for oxidizing may or may not be true for etching.

Moreover, claim 1 requires a trench having sidewalls, that are less resistant to etching, and sidewalls, that are more resistant to etching. A person skilled in art would not have

combined the teachings of Kudelka with those of Yasue since Yasue teaches away. In particular, Yasue expressly discloses that <100> sides are more desirable inside a trench than <110> sides (see paragraph [0019]) to avoid cracks in the wafer (see paragraph [0024]). According to the teachings of Yasue, a person skilled in the art would have certainly not chosen to build a trench which has different type of crystal sides within one trench since this would have increased the chance of having cracks in the wafer. Hence, independent claim 1 is allowable.

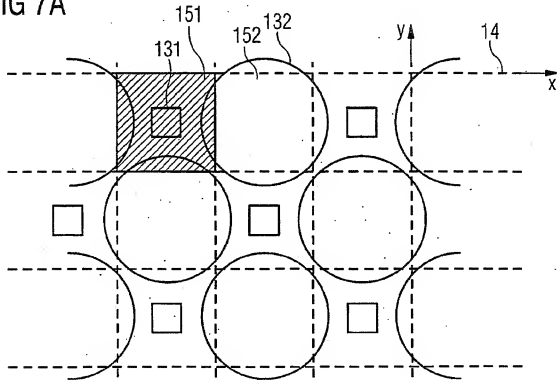
Claims 22-27 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 2, 7, 8, 11, 12 and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka in view of Sakao (U.S. Patent Publication No. 2001/0050436, hereinafter "Sakao"). Claim 3 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudleka and Sakao as applied to claims 2 and 21, and further in view of Yasue. Claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelko and Sakao as applied to claims 8 and 21, and further in view of Yasue. Claims 4, 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 21, and further in view of Endoh. Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka and Sakao as applied to claims 12 and 21, and further in view of Förster et al. (U.S. Patent No. 6,455,369, hereinafter "Förster"). Applicant respectfully traverses these rejections.

Claim 21 specifically recites "said structure size of said trench structures expanded along said crystal faces that are less resistant to etching *beneath said second areas for forming said secondary structures* by said area selective etching." Kudelka, either singly or in combination with Sakao, does not show such a method.

Rather, Kudelka shows a bottle type trench wherein the sidewalls of the upper portion of the trench 202 and the sidewalls of the lower portion 206 of the trench are arranged along the crystal face <110> (see paragraph [0044]; Figure 11, 15-16). However, Kudlka does not show the extension of the trench structures into second areas since the expansion into second areas would automatically eliminate minimum thickness of the intermediate walls (problem described in paragraph [0059] of the published application and Figure 7A reproduced below). Sakao is silent regarding expanding of trench structures.

FIG 7A



Hence, independent claim 21 is allowable.

Claims 2-13 depend from claim 21 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable

claim as well as for adding new limitations.

Claims 28 and 35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka in view of Sakao. Claim 29 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 28, and further in view of Förster. Claims 30 and 31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 28, and further in view of Yasue. Claims 32, 33 and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudleka and Sakao as applied to claim 28, and further in view of Endoh. Applicant respectfully traverses these rejections.

Claim 28, as amended, specifically recites "forming sidewalls of the upper portion of the trench structure in said first areas wherein the sidewalls are substantially parallel to the crystal faces that are less resistant to etching; and forming sidewalls of the lower portion of the trench structure wherein the sidewalls of the lower portion are substantially parallel to crystal faces that are more resistant to etching." Kudelka, either singly or in combination with Sakao, does not teach or suggest such a method.

Rather, Kudelka shows a bottle type trench wherein the sidewalls of the upper portion of the trench 202 and the sidewalls of the lower portion 206 of the trench are arranged along the crystal face <110> (see paragraph [0044]; Figure 11, 15-16) and that silicon surfaces are etched faster in <100> direction than in <110> direction (see paragraph [0044]). Sakao is silent regarding crystal faces. Nothing in Kudelka and Sakao teaches or suggests that the upper portion of the trench structure comprises sidewalls substantially parallel to crystal faces that are less resistant to etching and that the lower portion of the trench structure comprises sidewalls substantially parallel to crystal faces that are more resistant to etching. Hence, independent claim 28 is allowable.

Claims 29-35 depend from claim 28 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 36, 37, 38 and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudleka in view of Wang et al. (U.S. Patent No. 6,703,273, hereinafter "Wang"). Claims 40 and 41 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudleka and Wang as applied to claim 36, and further in view of Forbes et al. (U.S. Patent No. 5,907,170, hereinafter "Forbes"). Claims 42,43 and 44 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudelka and Wang as applied to claim 36, and further in view of Endoh. Applicant respectfully traverses these rejections.

Claim 36 has been amended with the limitations of claims 37 and 38. Claim 36 requires "etching the semiconductor substrate to form upper portions of the trench structures, the upper portions of the trench structures having side walls along the <100> crystal faces, etching the semiconductor substrate to form lower portions of the trench structures beneath the upper portions, the lower portions being wider than the upper portions and comprise a substantially rectangular shape with side walls parallel to the <110> crystal face." Kudelka or Wang, either singly or in combination, does not show such a method.

Kudelka shows trench sides along the <110> crystal face (see Figure 14-16). In others words, Kudelka shows trench sides along only one crystal face. Wang shows trench sides along <100> crystal face (see column 3, lines 18-21 and column 4, lines 31-34). In other words, Wang shows trench sides along only one crystal face. None of the references indicates that a trench should have sides along different crystal faces.

Moreover, trenches have been etched along the <100> crystal face and the <110> crystal

face at least since 1976 (see, for example, "Fabrication of Novel Three-Dimensional Microstructures by the Anisotropic Etching of <100> and <110> Silicon," Ernest Bassous, IEEE Transactions on Electron Devices, Vol. ED-25, No. 10. October 1978, a copy is provided herewith for the Examiner's convenience; U.S. Patent 3,962,052 assigned to Abbas et al.). However, the prior art does not teach or suggest etching one part of a trench along the <100> crystal face and another part of the same trench along the <110> crystal face even though there has been a constant struggle and a long felt need to increase capacitance by utilizing the volume of the semiconductor substrate. Accordingly, a person skilled in the art would not have combined the teachings of the two references to form a trench having sidewalls along the <100> crystal faces in one part and sidewalls along the <110> crystal faces in another part. Hence, independent claim 36 is allowable.

Claims 37 and 39-44 depend from claim 36 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's Attorney, at 972-732-1001, so that such issues may be resolved as expeditiously as possible. The Commissioner is hereby authorized to charge any fees that are due, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

10/28/06

Date

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Fabrication of Novel Three-Dimensional Microstructures by the Anisotropic Etching of (100) and (110) Silicon

ERNEST BASSOUS

Abstract—The anisotropic etching of single crystal silicon of (100) and (110) orientation in a solution of pyrocatechol, ethylene diamine, and water is reviewed and the fabrication of three novel types of microstructures is described in detail. Controlled etching of Si, which is required to fabricate devices with a predictable geometry depends on an accurately oriented, defect-free substrate, a well-defined and aligned pattern geometry, and rigorously clean etching conditions. Conventional IC processing methods were used to fabricate: 1) a high-precision circular orifice in a thin p^+Si membrane for use as an ink jet nozzle, 2) a multisocket miniature electrical connector with octahedral cavities suitable for cryogenic applications, and 3) multichannel arrays in (100) and (110) Si useful in various applications, e.g., charge electrodes, physical masks, and optical devices. To make some of these structures, a novel bonding technique to fuse silicon wafers with phosphosilicate glass films was developed.

Introduction

Anisotropic etching of single crystal silicon resulting from the differential etch rate of its crystallographic planes has been used to fabricate a variety of active and passive, three-dimensional device structures which include X-ray masks [1]-[6], optical waveguides [7]-[9], high-resolution patterns [10]-[14], nozzles [15]-[18], microtools [19], diodes [20], [21], bipolar and MOSFET circuits [22]-[27], electromechanical [28] and micromechanical [29], [30] devices. Preferential and nonpreferential etching techniques have also been used to fabricate a wide variety of surface structured devices [31]-[33]. In this paper the anisotropic etching of (100) and (110) oriented single crystal silicon is reviewed, and the fabrication of three types of novel device structures in (100) and (110) Si is described. The devices are 1) a high-precision nozzle useful in ink jet printing, 2) a multisocket miniature electrical connector for use at cryogenic temperatures, 3) multichannel array structures useful in a variety of applications. The last two types of devices were fabricated by employing a novel bonding technique which is compatible with silicon IC (integrated circuit) processing methods. The anisotropic etching solution which was used in fabricating the structures was first reported by Finne and Klein [34] and contained pyrocatechol $C_6H_4(OH)_2$, (P), ethylene diamine $NH_2(CH_2)_2NH_2$ (ED) and water.

The fabrication of precision three-dimensional microstructures by the anisotropic etching of Si is influenced by the following factors: a) the crystallographic perfection of the substrate, b) the geometry of the surface pattern which is delineated in an appropriate masking film on the substrate surface, and c) the control exercised over the anisotropic etching conditions. These factors will be discussed first, followed by a description of the fabrication of the ink jet nozzle, the electrical connector, and last, the multichannel arrays.

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Etching Behavior of (100) and (110) Oriented Silicon

Substrate

The etch rate of single crystal Si in an anisotropic etchant such as P-ED solution, varies with the crystallographic orientation of the substrate, and decreases, generally, in the order $(100) > (110) > (111)$. Cavities and mesas etched in Si wafers are bounded by sidewalls which represent the fastest and slowest etching planes of the crystal. To predict the geometry of these structures, in (100) Si for example, it is necessary to know the etch rates $R_{(100)}$ and $R_{(111)}$ of the (100) and (111) planes, respectively. In practice, the anisotropic etch rate ratio $R_{(100)}/R_{(111)}$ is first determined experimentally for a given device structure and this ratio is then used to establish device design parameters. A high and uniform value of $R_{(100)}/R_{(111)}$ enables the fabrication of small-geometry and high-density microstructures.

High-quality Si wafers of (100) orientation, accurately oriented within ±1° of their crystal axes, are readily available commercially in a wide range of diameter, thickness, surface finish, conductivity type, and resistivity. Wafers of (110) orientation are often of questionable quality and are not readily available due to their limited use in industry. Thermally grown SiO_2 was used almost exclusively as an etch mask because it is readily formed as a thin, uniform, defect-free film on clean Si surfaces regardless of the shape of the Si structure. SiO_2 is compatible with most device fabrication processes and its etch rate in P-ED is extremely low. SiO_2 films grown at 900–1100°C in steam, 0.5 to 2.0 μm thick were generally used in most processes.

The geometry of holes etched through openings in a surface oxide film is a function of the orientation of the Si substrate, the geometry of the opening, its alignment relative to the wafer's crystal axes, and the duration of etching. Fig. 1 illustrates the shape of three holes anisotropically etched in (100) Si through openings of different geometry in a surface masking film. After sufficient etching has occurred, the hole in the Si surface is a rectangle which encloses the opening in the surface masking film. The etched holes are bounded by four convergent {111} planes each of which makes an angle of 54.74°

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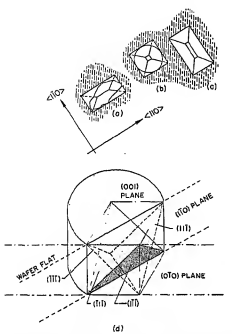

Fig. 1. Anisotropically etched holes through small openings of different geometry in a surface film on a (100) oriented silicon wafer. Four convergent self-limiting {111} etch planes define the sidewalls of each cavity. The geometry of the opening in: (a) arbitrary; (b) circular; and (c) rectangular. (d) The four sets of {111} planes in a (100) crystal are equivalent and intersect each other at the surface along the [110] directions.

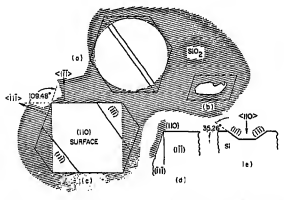

Fig. 2. Anisotropically etched holes through small openings of different geometry in a surface film on a (110) oriented silicon wafer. The exposed sidewalls inside each cavity are the {111} crystal planes of the wafer. The geometry of the opening in: (a) circular; (b) arbitrary; and (c) square; (d) two sets of {111} planes intersect the (110) surface vertically; (e) 2 other {111} planes intersect the surface at 35.26°.

(arctan $\sqrt{2}$) with the surface plane. The intersection of the {111} planes with the (001) surface in Fig. 1 are orthogonal, and are parallel or perpendicular to the [110] directions. A similar effect is observed with (110) oriented Si, but in this case the geometries of the etched holes are different due to the fact that the four sets of {111} planes which form the sidewalls of the cavities are not equivalent. As shown in Fig. 2 the (1$\bar{1}$1) and (1$\bar{1}\bar{1}$) planes are perpendicular to the (110) surface plane and intersect each other at the surface at an angle of 109.48°. The ($\bar{1}\bar{1}$1) and (11$\bar{1}$) planes intersect the (110) surface at an angle of 35.26°, and intersect each other inside the cavity at 109.48°. As a result, the etched hole in the Si surface is either a rhombus or a hexahedron depending on the size of the opening and the etching time.

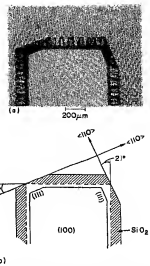

Fig. 3. Effect of 21° misalignment of a surface pattern relative to the <110> direction on the shape of an anisotropically etched hole in (100) Si. (a) Photomicrograph of the hole etched through a rectangular opening in a surface film of SiO_2. (b) Sketch of (a) showing the geometry of the hole pinned to the {111} planes at two corners, and underetching of the oxide opening on three sides.

Alignment

Accurate crystallographic alignment of the surface pattern which is required in order to achieve dimensional control during etching, is accomplished when the straight sides of openings are parallel to the intersections of the {111} planes with the accurately oriented surface plane. The pattern geometry for (100) Si should therefore be orthogonally defined on the wafer surface along the [110] directions. Designs based on this geometry are conventional in making photomasks for IC fabrication. For (110) Si, the surface pattern should be rhombohedral, and aligned parallel to the [111] directions as shown in Fig. 2. The latter geometry is usually much more difficult to design into a surface pattern using current photomask fabrication systems, and is therefore seldom adopted. The effect of misaligning an opening in an oxide film is to increase the size of the etched hole in the Si substrate. The increase in size is caused by underetching of the oxide opening which enlarges the hole until its geometry is pinned to the nearest {111} planes which enclose the oxide opening. The effect of a 21° misalignment on the geometry of an etched hole in (100) Si is shown in Fig. 3. This etching phenomenon can be put to practical use in establishing crystal orientation and in providing built-in alignment features for pattern registration. It is also useful for generating etched holes of different size by adjusting the alignment angle of the same oxide opening. For example, a small square opening, side W, in an oxide film on a (100) Si surface forms a square etched hole whose size ranges from W to $\sqrt{2}\ W$ as the angle is increased from 0° to 45° relative to the <110> direction. For any angle θ, the side dimension of the etched square hole in the Si surface is $W(\sin\theta + \cos\theta)$.

P-ED Etchant

Uniform and controlled etching was obtained with an etchant of the following composition: 4 m % (mol percent) pyrocatechol, 46.4 m % ethylene diamine, and 49.4 m % water. The solution was used at its boiling point 118 ± 1°C, in a nonoxidizing atmosphere, and its composition was maintained constant by means of a reflux condenser system [35]. The etch rates of the {100}, {110}, and {111} planes in P-ED are 50, 30, and 1 μm/h, respectively, based on measurements of etched cavities in (100) and (110) Si substrates. The etch rates of thermally grown SiO_2 and chemically vapor deposited Si_3N_4 films are 150 and 80 Å/h, respectively. The low etch rate of SiO_2 in this etchant is a distinct advantage in the fabrication of devices which require prolonged etching.

Due to the high etch selectivity of P-ED, residues or contaminants adhering to clean Si surfaces cause local masking and consequently nonuniform etching. Rigorously clean Si surfaces were thus necessary for the controlled etching of precision devices. Removal of the thin native oxide from Si surfaces in buffered HF prior to immersion in P-ED was also essential to ensure uniform etching and prevent hillock formation [36], [37]. Precipitates formed on Si surfaces after etching in P-ED were dissolved readily in buffered HF. P-ED was found to be stable and useful over periods of weeks provided the solution was kept in a nonoxidizing atmosphere and did not contain excessive amounts of Si. In a critical device application, etching control was best achieved with a fresh solution containing, if necessary, a higher percentage of ethylene diamine. The latter was required when occasional hillock formation persisted.

Fabrication of Microstructures

Nozzles

Arrays of nozzles of uniform size and spacing are required for the operation of ink jet printers using binary, deflected, electrostatically charged ink jets [38]-[41]. Two types of nozzles have been fabricated experimentally in (100) silicon which fulfill these requirements. The first is a pyramidal-shaped nozzle with a square orifice [16] which is formed by the anisotropic etching of holes through a (100) oriented Si wafer. The square orifice is defined by four convergent {111} planes which intersect the (100) surface of the wafer. In Fig. 4 examples are shown of discrete nozzles and arrays of nozzles with square orifices. The fabrication and performance of such devices in an experimental printer have been described elsewhere [18], [35]. The second type of nozzle is a circular orifice defined in a thin heavily doped p^+ Si membrane which is edge-supported in a pyramidal cavity etched in (100) Si [15].

Pyramidal-shaped holes for nozzle fabrication were etched in (100) Si wafers using patterns of different geometry. Openings in the SiO_2 film on the Si surface were square, circular, or open-cross, the last being a cross superimposed on a smaller square opening. The etched hole which was generated from a square opening was, as expected, identical in geometry to the opening itself provided it was aligned parallel to the <110> direction. A circular opening, however, yielded initially an octagonal-shaped hole in the Si surface. As etching pro-

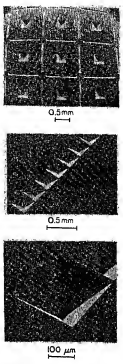

Fig. 4. SEM photomicrographs of ink jet printing nozzles etched in (100) silicon. (Top) 9 discrete nozzles on 1.2-mm centers on a silicon wafer. (Center) An array of 8 nozzles on 0.3-mm centers. (Bottom) Each nozzle is a truncated square pyramidal cavity 200 μm deep with an orifice 25 × 25 μm^2.

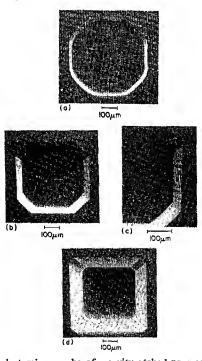

Fig. 5. SEM photomicrographs of a cavity etched progressively deeper into a (100) Si wafer through a circular opening in an SiO_2 surface film. Hole depth (a) 29 μm; (b) 60 μm; (c) a higher magnification of (b) showing multifaceted corners; (d) 120 μm. Corners eventually disappear to form a square hole in the Si surface.

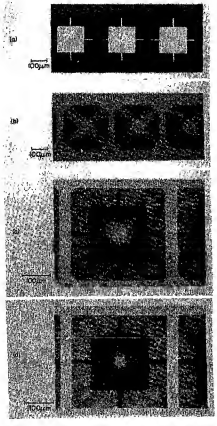

Fig. 6. Photomicrographs of an open-cross pattern etched progressively deeper into a (100) Si wafer through an SiO_2 etch mask. (a) Pattern geometry of three openings prior to etching. (b) Holes in silicon etched 120 μm deep. (c) Single hole etched 160 μm deep. (d) Hole 175 μm deep with a square base hole on the top surface and a square orifice etched through the opposite side of the wafer. The original surface pattern is clearly defined by the SiO_2 overhang.

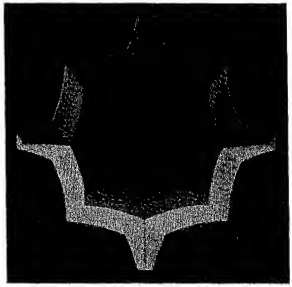

Fig. 7. SEM photomicrograph of an etched hole in a (100) Si surface using the open cross-pattern shown in Fig. 6. The oxide masking film is etched off to show the rapid etching and rounding of intersecting {111} planes at convex (mesa) corners and edges.

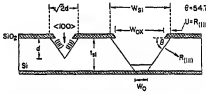

Fig. 8. Cross section through anisotropically etched pattern in (100) Si. The orifice dimension $W_o = W_{Si} - \sqrt{2}\, t_{Si}$, and the underetching U are a function of the etch rate $R_{(111)}$ of the {111} planes and etching time t for an accurately aligned pattern and a defect free Si-SiO_2 interface.

gressed into the substrate, four well-defined {111} planes developed and increased in size until the octahedral hole became a square as shown in the SEM photomicrographs of Fig. 5. Close examination of Fig. 5(c) reveals that the corners of the octagon are multifaceted and not discrete crystallographic planes as was reported with other anisotropic etchants [26], [36]. An open-cross pattern exhibited a similar etching behavior with respect to the development of self-limiting {111} planes as shown in Fig. 6. This occurred due to the rapid etching of convex (mesa) corners under the oxide opening during the initial stages of etching. Fig. 7 is a SEM photomicrograph of a multifaceted cavity etched 30 μm deep into a (100) Si substrate using the open-cross pattern of Fig. 6. It illustrates convincingly the difference in stability of intersecting {111} planes at convex (mesa) and concave (cavity) corners and edges in P-ED etchant. With any of the patterns just described, the final geometry of the etched hole was the same after sufficient etching had occurred. As shown in Fig. 8, the dimensions of a square pyramidal hole is given by the expression

$$W_o = W_{Si} - \sqrt{2}\ t_{Si}$$

where W_o is the side of the square apex or orifice, W_{Si} the side of the square base hole in the wafer surface, and t_{Si} the etched depth or wafer thickness. The underetching $U = R_{(111)}t/\sin\theta$ represents the difference between the oxide opening and the base hole in the Si surface. It is due to the small but finite etch rate of the {111} planes $R_{(111)}$, the etching time t, and the angle $\theta = 54.74°$ between the {111} planes and (100) surface.

Membrane-type nozzles with circular orifices were fabricated by etching holes as previously described, in combination with a process which takes advantage of the etch resistance of heavily doped p^+ Si in P-ED. At an impurity concentration $N_A \simeq 10^{19}$ cm^{-3} the etch rate of Si in P-ED drops sharply and reaches practically zero at $N_A \geq 7 \times 10^{19}$ cm^{-3} [42], [43]. When a silicon wafer with a heavily doped p^+ surface layer is etched in P-ED, the undoped Si is removed and a membrane is left whose thickness is equal to the depth of the surface layer with a concentration $N_A \geq 7 \times 10^{19}$ cm^{-3}. This property has been used to fabricate various device structures incorporating membranes ranging in thickness between 1 and 10 μm [1]-[5], [20], [21], [28]. This technique was also used to fabricate a high-precision orifice in a p^+ Si membrane for use as an ink jet printing nozzle. The fabrication process of this membrane

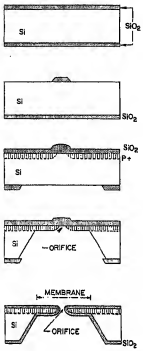

Fig. 9. Method of fabricating a silicon membrane nozzle using conventional processing techniques. The nozzle is a high-precision orifice defined in a thin heavily doped p^+ Si membrane. A (100) Si wafer is oxidized; an orifice pattern is defined on one side of the wafer followed by a heavy p^+(boron) diffusion, reoxidation, and opening of a base hole in the SiO_2 film on the opposite side. Anisotropic etching through the wafer proceeds along the {111} planes and the contour of the p^+ diffusion profile; finally, the SiO_2 masking film is stripped off and the wafer reoxidized.

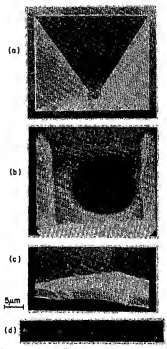

Fig. 10. Photomicrographs of Si membrane nozzles. (a) Discrete nozzle looking down the square base hole 0.4 × 0.4 mm^2 of the pyramidal cavity 0.2 mm deep. (b) Circular orifice ~20-μm diameter in a rectangular p^+ Si membrane 3 μm thick. (c) Cross section of an orifice showing the flared contour of the edge. (d) Five discrete nozzles on 0.6-mm centers viewed from the orifice side of the wafer.

nozzle is illustrated schematically in Fig. 9. A clean Si wafer of (100) orientation, chem-mechanically polished on both sides, either p-or n-type, 0.1–20 Ω · cm was thermally oxidized to grow an SiO_2 film 1–2 μm thick. This film served as a boron diffusion mask in the subsequent processing step. A thinner masking layer was sometimes employed by replacing the SiO_2 film with a dual layer of $SiO_2 + Si_3N_4$. An orifice pattern consisting of an array of circular SiO_2 dots was delineated photolithographically on one side of the wafer while protecting the SiO_2 layer on the opposite side. Each SiO_2 dot defined the geometry of the orifice in the final structure. A boron diffusion from a BBr_3 source was then carried out under conditions which resulted in a boron surface concentration close to its solubility limit in silicon. The thickness of the p^+ Si membrane in the final structure was equal to the region in the p^+ surface layer whose concentration $N_A \geq 7 \times 10^{19}$ cm^{-3}. In 10-Ω · cm Si, a junction depth 8 μm deep yielded a membrane approximately 3 μm thick. After diffusion, an SiO_2 film approximately 1 μm thick was thermally grown on the doped surface. A base hole pattern was delineated photolithographically on the other side of the wafer, and pyramidal holes were then etched through the substrate to form orifices in a membrane on the diffused side of the wafer. Excessive etching had no effect either on the p^+ Si membrane or on the size of the orifice, but the base hole increased slightly in size due to the small etch rate of the {111} sidewalls. As shown in Fig. 9, the orifice geometry is defined by the masked region on the wafer surface and by the boron diffusion junction. After P-ED etching was completed, the oxide layers on the front and back surfaces were stripped off, and a uniform SiO_2 film ~1 μm thick was thermally grown on all exposed Si surfaces of the nozzle. In the fabrication process, the registration of the orifice and base hole patterns and their respective alignment to the wafer's crystal axes were accomplished by the help of holes etched through the wafer prior to pattern definition. For more moderate registration accuracy, alignment features on the photomask, and mechanical adjustments on the optical exposure system were adequate. Nozzles with an orifice diameter ~20 μm, in a p^+ Si membrane 3 μm thick are shown in Fig. 10. The flared contour of the orifice edge, which is apparent in a cross section of the orifice, results from the boron diffusion profile under the edge of the SiO_2 orifice mask.

The geometry of the orifice in membrane nozzles is not restricted to circular openings but can be controlled by orifice pattern design and by the diffusion conditions. Orifice dimensions can be increased in small increments by isotropic etching or by oxidation and oxide stripping. Orifice dimensions in the submicrometer range using optically defined patterns are feasible by adjusting the diffusion time and thereby the lateral spread of the dopant under the orifice diffusion mask. Finally, multiple orifices on the same membrane formed on (100) and (110) Si could be fabricated as shown in Fig. 11.

Multisocket Electrical Connector

A miniature electrical connector for packaging electronic circuits which are required to operate at cryogenic temperatures, was fabricated by bonding two wafers possessing

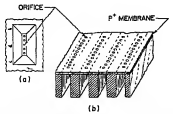

Fig. 11. Multiple orifices in a single p^+ Si membrane on (a) (100) Si wafer, and (b) (110) Si wafer using the fabrication method outlined in Fig. 9.

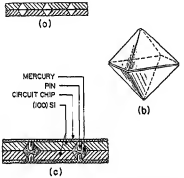

Fig. 12. Multisocket electrical connector for packaging cryogenic circuits is formed by bonding two identical wafers in which are etched pyramidal cavities. (a) Cross section of three cavities. (b) Each cavity is an octahedral structure formed of two nozzles with square orifices of the type shown in Fig. 4. (c) Mercury in the cavities serves as the electrically conductive medium in the final packaged circuits.

Fig. 13. SEM photomicrographs of a multisocket electrical connector. The cavities are on 1.3-mm centers, overall height 0.6 mm, square openings on opposite sides are 125 × 125 μm^2, opening at the center 0.45 × 0.45 mm^2. (a) Bonded, completed structure. (b) Cross section of an octahedral cavity. (c) Cross section showing {111} sidewalls of the upper and lower parts of the same cavity.

identical arrays of truncated pyramidal holes [44]. The resulting structure consisted of arrays of octahedral cavities with small square openings 125 × 125 μm^2 on opposite sides of the laminated wafers as shown in Fig. 12. In operation, the cavities are filled with a suitable, low-melting, conducting material such as mercury, which is retained inside the cavities at room temperature due to surface tension. Input and output signals from individual circuit elements are carried via pins which are inserted from opposite sides of the connector as shown in Fig. 12. The zero insertion force of this high-density demountable connector is one of its major attributes.

The fabrication of the connector employed the same techniques used for fabricating nozzles. Two identically processed silicon wafers with mirror-image nozzle array patterns were aligned and bonded with their base hole sides in contact to form the required octahedral cavities. The bonding process is a novel technique which takes advantage of the relatively low melting point of phosphosilicate glass (PSG) films, and of the ease with which thin uniform layers of PSG are formed on oxidized Si surfaces. After the nozzles were etched, the SiO_2 film which served as an etching mask was stripped off, and a new SiO_2 film 1–2 μm thick was then thermally grown on the wafers. A PSG layer containing approximately 10 percent P_2O_5 was formed on the SiO_2 surfaces by exposing the wafers to a mixture of phosphorus oxychloride $POCl_3$ vapor and O_2 gas at 900°C. The wafers were then aligned and clamped together inside a quartz vacuum-chuck assembly which forced the wafer surfaces into intimate contact by connecting it to a vacuum pump throughout the bonding process. The quartz assembly was introduced into a furnace at 1100°C and heated for 30 min, then slowly cooled to room temperature. Fusion of the PSG layers took place readily and the resulting bond strength was excellent provided the wafer surfaces were clean and reasonably flat. The completed bonded structure is shown in Fig. 13. Electrical connectors made by this process were cycled repeatedly between liquid nitrogen and room temperature without suffering structural failures.

Multichannel Arrays

Arrays of parallel trenches and channels with V-shaped and U-shaped cross sections, as shown in Fig. 14, were fabricated by etching long rectangular openings in (100) and (110) Si, respectively. Control of channel width and spacing was critically dependent on accurate wafer orientation and pattern alignment as well as on the use of defect free substrates. Misalignment generated sidewall imperfections and caused merging between adjacent channels especially in long dense structures. The nature of the imperfections in the sidewalls of vertically etched grooves in (110) Si has been discussed by Kendall [14]. The arrays of V-shaped trenches shown in Fig. 14(a) and (b) were used in making optical waveguides [8]. The structure shown in Fig. 14(c) consists of eight equally spaced rectangular slots 200 μm wide with vertical sidewalls etched in a (110) Si wafer 200 μm thick. Structures such as this, have been used as charge electrodes in ink jet printing [45], as physical masks for evaporation and reactive ion etching, and in the fabrication of a multiprobe electrical connector for use at cryogenic temperatures. The latter was fabricated by sawing symmetrically

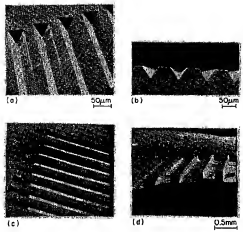

Fig. 14. Anisotropically etched channels in single crystal silicon. (a) (100) orientation. (b) Cross section of (a). (c) Bars and slots 200 μm wide with vertical sidewalls etched through a (110) Si wafer 200 μm thick. (d) Parallel trenches etched in (110) Si.

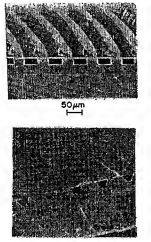

Fig. 15. Cross sections of enclosed arrays of channels formed by fusing the surfaces of two silicon wafers with phosphosilicate glass films. One surface is planar and the other surface has parallel trenches etched in a (110) Si wafer (top) and a (100) Si wafer (bottom).

across an array of slots, forming thereby, two identical in-line, multiple probe structures. Electrically conducting regions were formed by conventional diffusion and metallization techniques. Using the PSG bonding method described above, enclosed channel structures were also fabricated by laminating pairs of etched and planar silicon wafers. Cross sections obtained by cleaving such structures are shown in Fig. 15.

In conclusion, the three-dimensional microstructures described in this paper are bulk and surface structured devices whose geometry is dictated by the crystallography of the silicon substrate and the anisotropic etching characteristics of P-ED solutions. The self-limiting geometry is an advantage in fabricating predictable device structures with a high degree of precision. Where such a limitation is too restrictive, anisotropic and isotropic etching techniques could be used in combination to extend the range of device geometry. The use of thin silicon wafers also limits the geometry to structures which can be fabricated by processing the two surfaces of the substrate. Such a limitation is not inherent in the crystal structure of the substrate itself; in fact, the cubic symmetry of single-crystal silicon makes it a natural candidate for the fabrication of three-dimensional microstructures in a polyhedral substrate. The bonding technique which utilizes thin PSG films to fuse silicon wafers is also applicable to silicon-coated substrates and to silicate glasses which are capable of withstanding elevated temperatures. By fusing several discrete components made from these materials, complex, multifunctional, three-dimensional structures could be fabricated.

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Anisotropic Etching of Silicon

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Abstract—Anisotropic etching of silicon has become an important technology in silicon semiconductor processing during the past ten years. It will continue to gain stature and acceptance as standard processing technology in the next few years. Anisotropic etching of (100) orientation silicon is being widely used today and (110) orientation technology is emerging. This paper discusses both orientation-dependent and concentration-dependent etching of (100) and (110) silicon. Very exact process control steps may be designed into a process by use of (100) anisotropic and concentration-dependent etching. Also, methods of oxide or nitride pin hole detection in (100) silicon are presented. Mask alignments to obtain different etch front termination in both (100) and (110) silicon are shown. Very high packing density structures, less than 1 μm, are obtained in the (110) technology, and extremely high etching ratios of greater than 650 to 1 are obtained in (110) orientation-dependent etching. Some of the many applications for anisotropic and concentration-dependent etching are described.

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Orientation-Dependent Etching

WET CHEMICAL ETCHING has been used in silicon semiconductor processing since its beginning in the early 1950's. Isotropic etches, i.e., etches that etch in all crystalographic direction at the same rate, consisting of hydro-

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